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09/660,484	09/12/2000	Yasuo Tanaka	OKI 262	6834

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EXAMINER

FOONG, SUK SAN

ART UNIT

PAPER NUMBER

2823

#6

DATE MAILED: 05/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/660,484

Applicant(s)

TANAKA, YASUO

Examiner

Suk-San Foong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 07 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1, and 3-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, and 3-15 is/are rejected.
- 7) ☒ Claim(s) 1 and 6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 1, line 3, it appears that "plurality of semiconductors" should be replaced by-- plurality of semiconductor devices--.
2. Claim 6 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The recitation of claim 6 requires the step of claim 1, lines 9-10, as the sheet encapsulating material is heated and cured at a curing temperature to form encapsulating resin layer.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:  

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
4. Claims 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
5. Claims 7-9, the use of "predetermined" reads on a nebulous mental step conducted prior to the manipulative steps of the claimed invention, hence rendering the present process claims

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unclear in meaning and scope. If applicant wishes to patent detailed controls over the recited process, they must be positively recited.

6. Claims 7-9, it is questioned what is recited through the use of the term “easy”.
7. Claim 8, line 6, it is questioned what is recited through the use of the term “reduced”.
8. Claim 9, it is unclear what temperature range is recited through the use of “void removal temperature”.

***Claim Rejections - 35 USC § 102***

9. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 3, 4, 6, 11, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Chakravorty ('569).

Chakravorty teaches a method of forming plurality of metal bumps on semiconductor wafer which includes providing wafer 301 with plurality of integrated circuit (IC) chips 302 (Col. 7, lines 45-47, and Fig. 2), forming contact pads 304 on IC chips 302 (Col. 7, lines 49-54), then forming metal layers 307 and 310 to electrically connect to contact pads 304 (Col. 8, lines 32-56), depositing metal bumps 311-1 over metal layer 310 (Col. 8, lines 57-61 and Fig. 5A) and optionally reflowed to form partial spherical bumps 311 as shown in Fig. 5B (Col. 9, lines 31-54), subsequently encapsulating wafer 301 with encapsulant layer 312 such as epoxy resin,

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polyimides or polymeric materials (Col. 9, line 55 to Col. 10, line 7), then baking wafer 301 (Col. 9, line 65 to Col. 10, line 7) in order to cure and dry encapsulant layer 312 (Col. 12, lines 57-60), then polishing encapsulant layer 312 to expose top portions of bumps 311 (Col. 11, lines 1-12), then forming external terminals 314 over bumps 313 (Col. 11, lines 19-25, and Fig. 8D), and dividing wafer 301 into individual chips (Col. 12, lines 21-22)

***Claim Rejections - 35 USC § 103***

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims 1, 5, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilleo et al. ('058) in combination with Chakravorty ('569).

Gilleo et al. teach a method of forming encapsulant over semiconductor wafer which includes providing a semiconductor wafer 12 with bumps 14 (Paragraph [0040] and Fig. 1), then providing encapsulant sheet containing thermoset resin (Paragraph [0022]), further applying the encapsulant sheet onto the wafer (Paragraph [0028]), subsequently heating the encapsulant sheet to bond with wafer (Paragraph [0028]), and dicing the wafer to produce individual chips (Paragraph [0032]).

Gilleo et al. does not teach polishing encapsulant sheet to partially expose solder bumps 14.

Chakravorty teaches a method of forming plurality of metal bumps on semiconductor wafer which includes providing wafer 301 with plurality of integrated circuit (IC) chips 302

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(Col. 7, lines 45-47, and Fig. 2), forming contact pads 304 on IC chips 302 (Col. 7, lines 49-54), then forming metal layers 307 and 310 to electrically connect to contact pads 304 (Col. 8, lines 32-56), depositing metal bumps 311-1 over metal layer 310 (Col. 8, lines 57-61 and Fig. 5A) and optionally reflowed to form partial spherical bumps 311 as shown in Fig. 5B (Col. 9, lines 31-54), subsequently encapsulating wafer 301 with encapsulant layer 312 such as epoxy resin, polyimides or polymeric materials (Col. 9, line 55 to Col. 10, line 7), then baking wafer 301 (Col. 9, line 65 to Col. 10, line 7) in order to cure and dry encapsulant layer 312 (Col. 12, lines 57-60), then polishing encapsulant layer 312 to expose top portions of bumps 311 (Col. 11, lines 1-12), then forming external terminals 314 over bumps 313 (Col. 11, lines 19-25, and Fig. 8D), and dividing wafer 301 into individual chips (Col. 12, lines 21-22)

It would have been within the scope to one ordinary skill in the art to combine both teachings to employ the polishing step of Chakravorty to expose bumps on semiconductor wafers because it would enable partial exposure of bumps 14 on semiconductor wafer 12 through polishing and further advantage of lowering assembly costs (Col. 4, lines 46-48).

With respect to claim 10, it is inherent that the sheet would not contact the wafer at all points at the same time due at least to local thickness variation of the encapsulant sheet and the topography of the wafer. Alternatively, the disclosure placing the encapsulant sheet would suggest one in the ordinary skill of the art successively placing the sheet because of the limited number of methods of placing the sheet encompassed by the disclosure of placing the sheet discussed above in Gilleo et al. (See MPEP 2131.02 and 2144.08).

In regard to claim 5, prior heating of wafer one or more times before application of the encapsulant as encompassed in claim 5, would be a matter of design choice because such a step

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does not solve any disclosed problem or provide any advantages. It appears the process could be performed equally well with or without prior heating of wafer.

12. Claims 7, 8, 9, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chakravorty ('569) as applied to claims 1, 3, 4, 6, 11, 12, and 13 above.

The heating step recited in claims 7 and 8 would be performed during the process of heating the resin to the curing temperature. The step recited in lines 9-10 would be obtained as the same materials are being treated the same as the instant invention.

Examiner takes official notice that it was known at the time of applicant's invention to coat semiconductor substrates having bump electrodes with resin at a reduced pressure followed by raising the pressure to achieve uniform coatings including reduction of voids.

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable the step of heating encapsulant sheet at reduced pressure followed by raising the pressure and further advantage of reducing voids in encapsulant sheet.

With respect to claim 14, Examiner takes official notice that use of sheet encapsulating material containing a curing agent enclosed in capsule to be broken at a curing temperature was known prior to applicant's invention.

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable the step of forming encapsulant sheet with curing agent enclosed in capsule.

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With respect to claim 15, Examiner takes official notice that use of sheet encapsulant material containing an antifoaming agent for removal of void was known prior to applicant's invention.

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable the step of forming encapsulant sheet with antifoaming agent.

*Conclusion*


13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

SF  
May 19, 2002

  
George Hourson  
Primary Examiner  
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